REMARKS

Claims 1-31 are pending in the application. Claims 1, 5, 8, 16, 19, and 22 are independent. No claims have been amended, canceled, or added.

Rejection of Claims 1-4 and 30-31 Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.6,396,116 to Kelly et al. (hereinafter "Kelly") in view of U.S. Patent No.5,558,928 to DiStefano et al. (hereinafter "DiStefano"). To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. (MPEP §2143) Applicant respectfully traverses the rejection.

Independent claim 1 recites in pertinent part "a first wafer having a first layer of bulk silicon, ***a first layer of active silicon*** disposed on the first layer of bulk silicon, a first layer of interconnects disposed on the first layer of active silicon, and a first metal pattern disposed on a top surface of the first layer of interconnects; a second wafer having a second layer of bulk silicon, a second layer of active silicon disposed on the second layer of bulk silicon, a second layer of interconnects disposed on the second layer of active silicon, and a second metal pattern disposed on a top surface of the second layer of interconnects, ***wherein the first wafer turned upside down***; and an interposer disposed between the top surface of the first metal pattern and the top surface of the second metal pattern, the interposer having a pattern of metal vias disposed in a cured thermosetting plastic, the pattern of metal vias being aligned with and electrically coupled to the first metal pattern and the second metal pattern, ***wherein the first wafer is bonded to the second wafer face-to-face using the interposer***" (emphasis added).

In the Office Action, the Examiner states that Kelly teaches at Figure 2 and column 4, lines 44-55 "a first wafer having a first layer of bulk silicon, a first layer of active silicon disposed on the first layer of bulk silicon, a first layer of interconnects disposed on the first layer of active silicon and a first metal pattern disposed on a top surface of the first layer of

interconnects" and at Figure 2, column 3, lines 7-17, column 5, lines 5-15, and column 5, lines 60-65 "a second wafer having a second layer of active silicon disposed on the second layer of bulk silicon, a second layer of interconnects disposed on the second layer of active silicon, and a second metal pattern disposed on a top surface of the second layer of interconnects." Applicant respectfully disagrees with the Examiner's characterization of Kelly.

Kelly appears to be directed to packaging optical sensor devices. The problem addressed in Kelly is that conventional ball grid array (BGA) methods of mounting and packaging components are not suitable for light-sensitive components such as optical sensors. The solution proposed in Kelly is to flip-chip bond the optical sensor formed on a first substrate to a second substrate.

Applicant respectfully submits that Kelly fails to teach or fairly suggest, among other things, a first layer of ***active silicon*** disposed on the first layer of bulk silicon as asserted by the Examiner. If the Examiner is asserting that it is inherent that the optical sensor is made from active silicon, Applicant respectfully reminds the Examiner that to establish inherency, an Examiner must provide rationale or evidence tending to show inherency. MPEP §2112 IV. If relying on extrinsic evidence, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. (MPEP §2112IV *citing In re Oelrich*, 666 F.2d 578, 581-582 (CCPA 1981)). If relying on rationale, an Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art (emphasis in original). (MPEP §2112IV *citing Ex parte Levy*, 17 USPQ.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Assuming, for the sake of argument, that one could conclude that the optical sensor is made from active silicon, it does not necessarily flow from the teachings of Kelly that the optical sensor is made from active silicon. For example, many optical sensors are made from germanium (Ge), indium gallium arsenide (InGaAs), lead sulfide (PbS), or other material. Accordingly, Applicant respectfully submits that the Examiner has failed to meet the burden of showing that

the optical sensor being made from active silicon is inherent in Kelly and therefore has failed to show where this element of independent claim 1 is taught or suggested by Kelly.

The Examiner concedes that Kelly fails to teach an interposer disposed between the top surface of the first wafer and the top surface of the second layer of interconnects, wherein the first wafer turned upside down, and the interposer having a pattern of metal vias disposed in a cured thermosetting plastic, but cites DiStefano for this proposition. That is, the Examiner states that DiStefano teaches an interposer disposed between the top surface of the first wafer and the top surface of the second layer of interconnects, wherein the first wafer turned upside down, the interposer having a pattern of metal vias disposed in a cured thermosetting plastic. The Examiner then concludes that it would have been obvious to dispose DiStefano's interposer between the top surface of the first wafer and the top surface of the second layer of interconnects, wherein the first wafer turned upside down, the interposer having a pattern of metal vias disposed in a cured thermosetting plastic in Kelly's device. The motivation for such a combination, the Examiner states, "is to form a unitary mass and cause the flowable dielectric material to flow and conform to the major surface of the circuit panels the pattern of metal vias being aligned with and electrically coupled to the first metal pattern and the second metal pattern and to cross link the material of the thermosetting plastic wherein the first wafer is bonded to the second wafer face to face using the interposer. Applicant respectfully disagrees with the Examiner's motivation to combine Kelly with DiStefano.

Any motivation to combine reference teachings must be found in the prior art of record. For example, an Examiner may find the suggestion or motivation to combine teachings in a reference (e.g., a U.S. Patent, inherency), in common knowledge in the art (i.e., well-known art), in established scientific principles, in art-recognized equivalents, or in legal precedent (e.g., admitted prior art). However an Examiner may not use an improper rationale for combining reference teachings. (MPEP §2145.) One such impermissible rationale is that if the proposed modification or combination of references would change the principle of operation of a reference, then such combination or modification may not be used to render the claimed invention obvious. MPEP §2143.01 (citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Applicant

respectfully submits that if Kelly were combined with DiStefano as suggested by the Examiner, DiStefano would change the principle of operation of Kelly.

For example, Kelly uses two substrates, the first of which has contact pads on the top surface and the second of which has contact pads on the bottom surface. A solder ball is placed between the contact pads on each substrate. Applicant respectfully submits that if the first substrate in Kelly were bonded face-to-face to the second substrate as suggested by the Examiner, then this would change the principle of operation of Kelly. For instance, the contact pad 214 on the second substrate would not be facing the contact pad 210 of the first substrate. There would be nothing for the solder ball 226 to join with. Thus, the first substrate and the second substrate could not be mounted and packaged together as required by Kelly.

Applicant respectfully submits that Kelly and/or DiStefano either separately or in combination fail teach or suggest each and every element of claim 1 because both fail to teach a first layer of active silicon. Applicant also respectfully submits that there is no proper motivation to combine Kelly with DiStefano to arrive at claim 1 because such a combination would change the principle of operation of Kelly. Applicant respectfully submits therefore that claim 1 is not obvious in light of Kelly in view of DiStefano. Because claim 1 is not obvious in light of Kelly in view of DiStefano, Applicant respectfully submits that claim 1 is patentable over Kelly in view of DiStefano and respectfully requests that the Examiner reconsider and remove the rejection to claim 1.

Claims 2-4 and 30-31 properly depend from claim 1, which Applicants respectfully submit is patentable. Accordingly, Applicant respectfully submits that claims 2-4 and 30-31 are patentable for at least the same reasons that claim 1 is patentable. (MPEP §2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 1-4 and 30-31.

CONCLUSION

Applicants submit that all grounds for rejection have been properly traversed, accommodated, or rendered moot, and that the application is in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Jan Little-Washington
Reg. No.: 41,181
(206) 292-8600

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